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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,444	12/31/2003	Jeung-Hie Choi	51876P555	1775

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
LUI, DONNA V	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,444	CHOI, JEUNG-HIE	
	Examiner	Art Unit	
	Donna V. Lui	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. **Claim 9** is objected to because of the following informalities: Claim 9 should be dependent upon claim 8. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claim 7** recites the limitation "the X and the Y address decoders " in line 2. Claim 6 recites having either an X or a Y address decoder while dependent claim 7 has both an X and Y address decoder. There is insufficient antecedent basis for this limitation in the claim.

4. **Claim 9** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 9 recites the limitation "...a clock frequency of the DC/DC booster is adjusted and the size of a transistor of the DC/DC booster is reduced in case of operating a large display panel of the display panels ...". The language implies a cause and effect relationship and the examiner is not sure if the size of a transistor is reduced at the time of manufacturing or through

the selection of different sized display panels, which implies that a different sized transistor may be used for varying panel sizes.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1 and 5** are rejected under 35 U.S.C. 102(e) as being anticipated by Kurashima et al. (Pub. No.: US 2003/0063041 A1).

With respect to **Claim 1**, Kurashima discloses a display apparatus *(See figure 1)*, comprising a plurality of display panels *(See figure 3, elements 3A and 4A)*, each showing different displays *([0010])*, a single display panel driving unit for commonly operating the display panels *(See figure 3, single display panel driving unit: IC 7; [0074], lines 5-9)*, and a connection means for physically and electrically inter-connecting the display panel driving unit with the display panels *(figure 3, connection means: element 8b; [0059], lines 7-9)*.

With respect to **Claim 5**, Kurashima discloses the display apparatus as recited in claim 1, wherein the display panel driving unit further comprises a display path control unit *(Kurashima teaches the display panel driving unit also functions as a display path control unit; [0087])* for

controlling a path connected with a display panel drive pad of a selected display panel in order to operate the selected display panel.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima.

With respect to **Claim 3**, the display apparatus as recited in claim 1. Kurashima does not teach the connection means is formed using a tape carrier package method. Official Notice is taken that both the concept and the advantages of providing for displays connection means formation using a tape carrier package method in display apparatus' are well known and expected in the art. It would have been obvious to have connections means formed using a tape carrier package method in Kurashima as these formation methods are known to provide reduced pitch, thin package profiles, and smaller footprint on the printed circuit board without compromising performance.

7. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima and Anila et al. (Patent No.: Us 6,583,770 B1).

With respect to **Claim 2**, Kurashima discloses the display apparatus as recited in claim 1, wherein the display panels includes a first display panel *(See figure 3, element 3A)* and a second display panel *(element 4A)*, and rear sides of the first and second display panels face each other *([0063])*. Kurashima does not teach the display panel driving unit disposed between the first and the second display panels.

Antila teaches a display panel driving unit *(See figure 3, element Dr)* disposed between the first *(element D1)* and second *(element D2)* display panels.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a display panel driving unit disposed between a first and second display panel, as taught by Antila, to the display apparatus of Kurashima so as to reduce the wire connections since the two displays are closer to the diver circuit.

8. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima as applied to claim 1 above, and further in view of Toba (Pub. No.: US 2002/0137551 A1).

With respect to **Claim 4**, Kurashima discloses the display apparatus as recited in claim 1. Kurashima does not teach the display panel driving unit comprises a plurality of display panel drivers for operating each of the display panels and a switching unit for switching the display panel drivers.

Toba teaches the display panel driving unit comprises a plurality of display panel drivers *(See figure 3, elements 25 and 26)* for operating each of the display panels and a switching unit *(element 21; [0052], lines 1-4)* for switching the display panel drivers.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have the display panel driving unit comprise a plurality of display panel drivers for operating each of the display panels and a switching unit for switching the display panel drivers, as taught by Toba, to the display apparatus of Kurashima, so as to provide a mobile communication terminal that can display data relating to the reception of a call, e-mail, or data of the received call on a main display or external display unit *(Toba: [0016])*.

9. **Claims 6-9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima as applied to claim 1 above, and further in view of Kou (Patent Number: 5,874,928).

With respect to **Claim 6**, Kurashima discloses the display apparatus as recited in claim 5, Kurashima does not mention the display panel driving unit further comprises a CPU interface control unit for controlling constitution elements included in the display panel driving unit by receiving a command from an external host or a central processing unit, a display panel control unit for controlling the display panel with an external control signal transmitted through the CPU interface control unit or an independent port, a memory unit for storing data displayed on the display panels, an X or an Y address decoder for selecting a corresponding address of the memory unit by decoding an encoding signal outputted from the display panel control unit, a register unit for informing each independent operation condition of the display panels, a timing control unit for controlling a point of time for decoding, latching and displaying a data for the selected display panel by the information obtained from the register unit, a line address decoder for decoding an address for the data of the corresponding display panel at a line unit by

responding to an output of the timing control unit, a latch unit for latching the data corresponding to the address decoded at the line unit, wherein the data is transferred from the memory unit, and a voltage generation unit for supplying a power voltage for operating each display panel.

Kou teaches a CPU interface control unit *(See figure 2, element 30)* for controlling constitution elements included in the display panel driving unit by receiving a command from an external host *(host computer; column 5, lines 38-40)*, a display panel control unit *(element 32; column 5, lines 57-62)* for controlling the display panel with an external control signal transmitted through the CPU interface control unit or an independent port, a memory unit for storing data displayed on the display panels *(element 36)*, an address decoder *(column 5, lines 43-49; note that the address decoder maybe a an X, Y or X and Y address decoder)* for selecting a corresponding address of the memory unit by decoding an encoding signal outputted from the display panel control unit, a register unit *(element 40: data serializer is equivalent to the register unit; column 6, lines 49-59)* for informing each independent operation condition of the display panels, a timing control unit *(element 58; column 7, lines 44-52)* for controlling a point of time for decoding, latching and displaying a data for the selected display panel by the information obtained from the register unit, a line address decoder for decoding an address for the data of the corresponding display panel at a line unit by responding to an output of the timing control unit *(please note again column 5, lines 43-49; In order to be able to provide data to the display panel where each row is scanned it is necessary to have a line address decoder for decoding an address for a particular row)*, a latch unit *(note that the latch unit is equivalent to input/output buffers; column 5, lines 47-49)* for latching the data corresponding to the address decoded at the line unit, wherein the data is transferred from the memory unit, and a voltage generation unit

(element 60: power controller is equivalent to the voltage generation unit) for supplying a power voltage for operating each display panel *(column 9, lines 65-67; column 10 lines 1-3 and lines 7-9).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a CPU interface control unit, a display panel control unit, a memory unit, an address decoder, a register unit, a timing control unit, a line address decoder, a latch unit, and a voltage generation unit, as taught by Kou, to the display apparatus of Kurashima, so as to provide a mechanism for simultaneously driving a plurality of displays which refreshes each of the displays at an optimal refresh rate for that display *(Kou: column 4, lines 41-44)* and to improve performance of both displays *(Kou: column 4, lines 45-46).*

With respect to **Claim 7**, Kurashima discloses the display apparatus as recited in claim 6, please note the above 35 U.S.C 112 2nd rejection. Kurashima does not mention the display panels share the X or Y address decoders, the line address decoder, the voltage generation unit, the memory unit and register unit during a concurrent and cooperative operation.

Kou teaches the shared X or Y address decoders, shared line address decoder, shared voltage generation unit, shared memory unit and a shared register unit during concurrent and cooperative operation *(column 4, line 62 to column 5, line 11; note that the drive signals are provided to a plurality of displays by one controller, the controller being element 16: display controller).*

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have shared X or Y address decoders, a shared line address decoder, a

shared voltage generation unit, a shared memory unit and a shared register unit during concurrent and cooperative operation, as taught by Kou, to the display apparatus of Kurashima, so as to provide a mechanism for simultaneously driving a plurality of displays which refreshes each of the displays at an optimal refresh rate for that display *(Kou: column 4, lines 41-44)* and to improve performance of both displays *(Kou: column 4, lines 45-46)*.

10. **Claims 8 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurashima in view of Kou as applied to claims 1, 5, and 6 above, and further in view of Nikawa et al. (Pub. No.: US 2002/0111200 A1).

With respect to **Claim 8**, Kurashima discloses the display apparatus as recited in claim 6. Neither Kurashima nor Kou teach the voltage generation unit comprises a voltage converter and a DC/DC booster controlled by on-off states of the first and second display panels.

Nikawa teaches a voltage generation unit *(See figure 4, element 27)* comprising a voltage converter *([0032])* and a DC/DC booster.

Nikawa modifies the display apparatus of Kurashima and Kou by replacing the power controller of Kou with the power source of Nikawa such that the voltage generation unit is controlled by the on-off states of the first and second display panels of Kurashima *(note that the on-off states are equivalent to whether a scanning signal is supplied to a display of Kurashima: [0087])*.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a voltage generation unit comprised of a voltage converter and a

DC/DC booster controlled by on-off states of the first and second display panels, as taught by Nikawa, to the display apparatus of Kurashima as modified by Kou, so as to eliminate unnecessary power consumption and to provide maximum operating efficiency *([0015])*.

With respect to **Claim 9**, Kurashima discloses the display apparatus as recited in claim 9. In light of the above 35 U.S.C. 112 2nd rejection, the examiner did not consider the limitation regarding a transistor due to the indefiniteness of how the size of a transistor is reduced. Kurashima does not mention a clock frequency of the DC/DC booster is adjusted and an output state of the memory unit or the address decoder is decided according to on-off operation states of the first and the second display panels and consequently, the memory unit is partially accessed.

Nikawa teaches a clock frequency of a DC/DC converter is adjusted *([0042])*. By replacing the voltage generation unit of Kurashima, as modified Kou with that of Kikawa, the display apparatus achieves the result of an output state of the address decoder is decided according to on-off operations states of the first and the second display panels. In order for the display to function properly, the on-off states of the first and second display panels decide the output state of the address decoder, namely if a line needs to be decoded.

It would have been obvious for a person of ordinary skill in the art at the time the invention was made to have a clock frequency of a DC/DC converter adjusted such that an output state of the address decoder is decided according to on-off operation states of the first and the second display panels, as taught by Nikawa, to the display apparatus of Kurashima so as to eliminate unnecessary power consumption and to provide maximum operating efficiency *([0015])*.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna V. Lui whose telephone number is (571) 272-4920. The examiner can normally be reached on Monday through Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571)272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Donna V Lui
Examiner
Art Unit 2629

AMR A. AWAD
PRIMARY EXAMINER